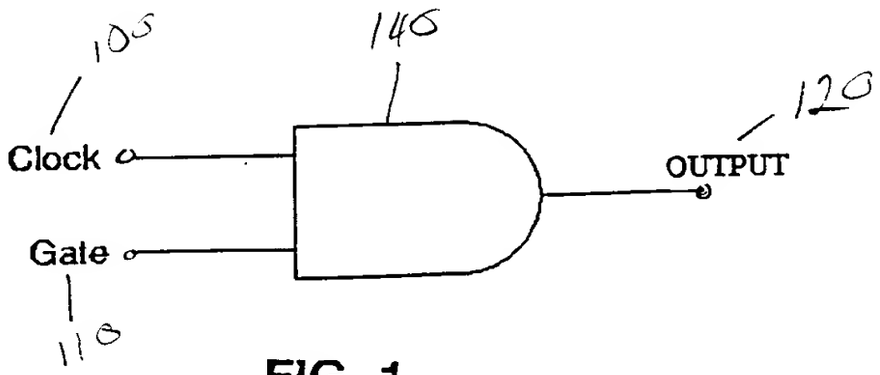

FIG. 1

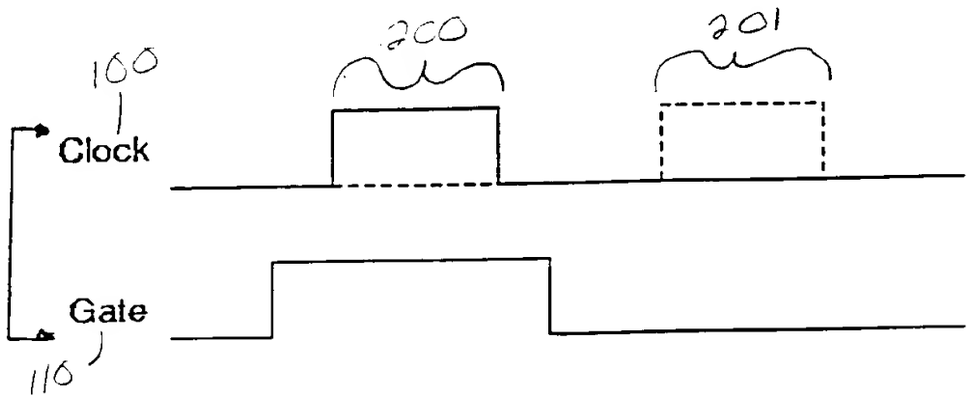

FIG. 2

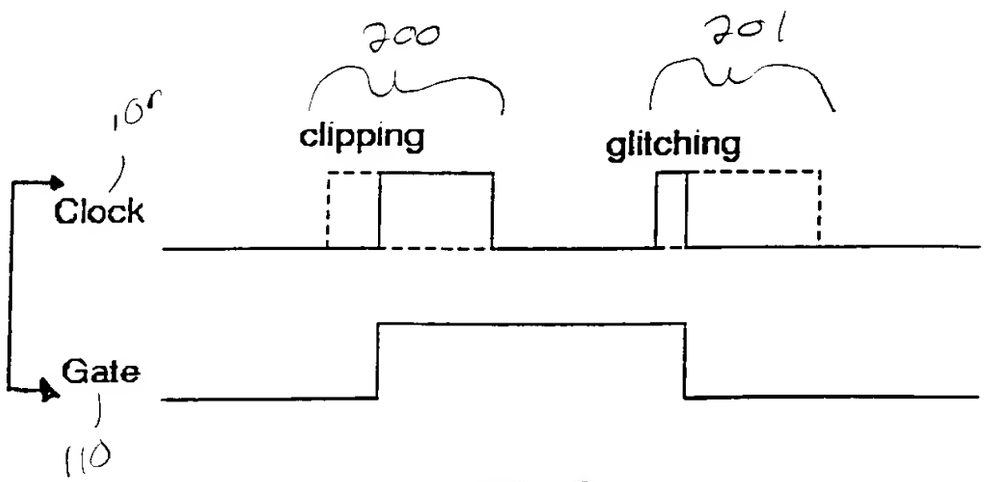

FIG. 3

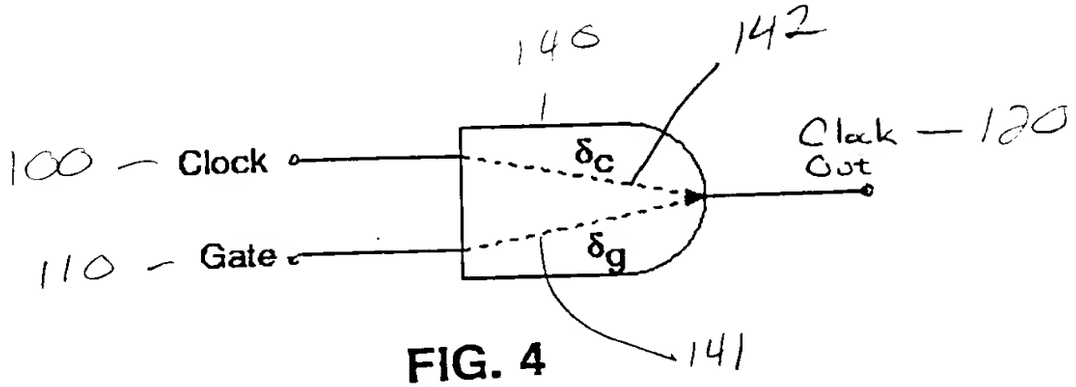
140
142
100 — Clock
110 — Gate
δ_c
δ_g
Clock Out — 120
141

FIG. 4

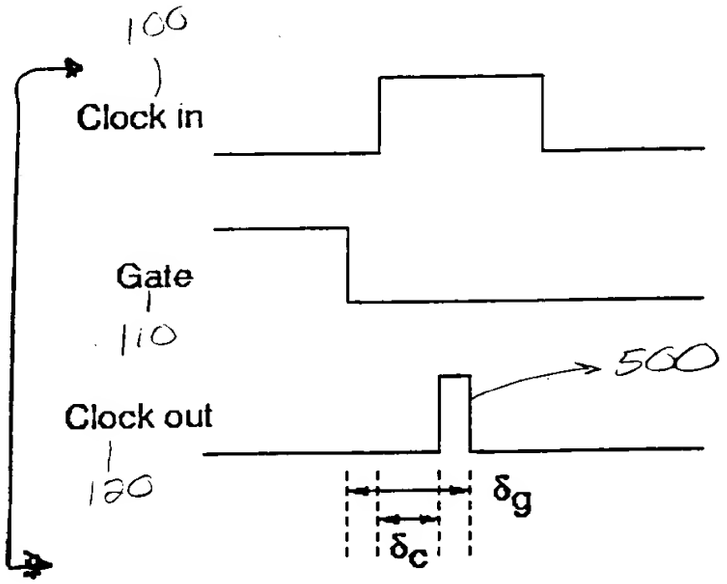
100
Clock in
Gate
110
500
Clock out
120
δ_g
δ_c

FIG. 5

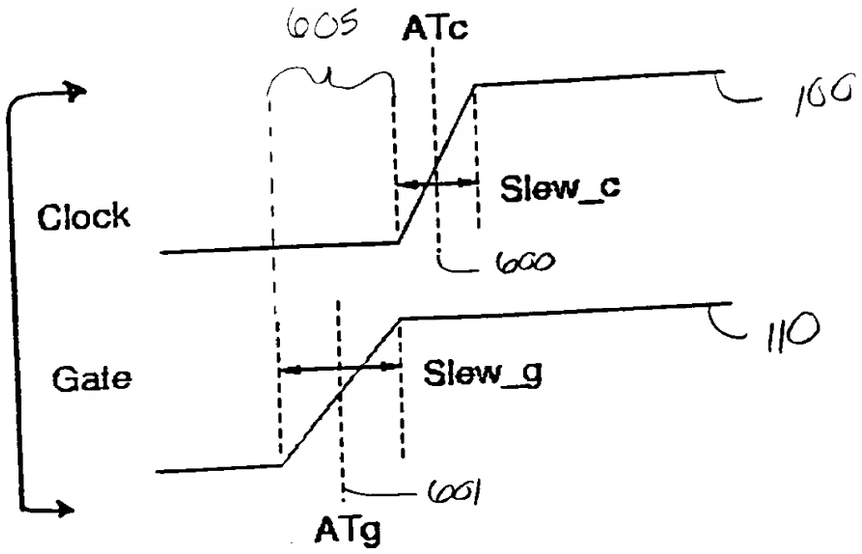
605
ATc
100
Clock
Slew_c
600
110
Gate
Slew_g
601
ATg

FIG. 6A

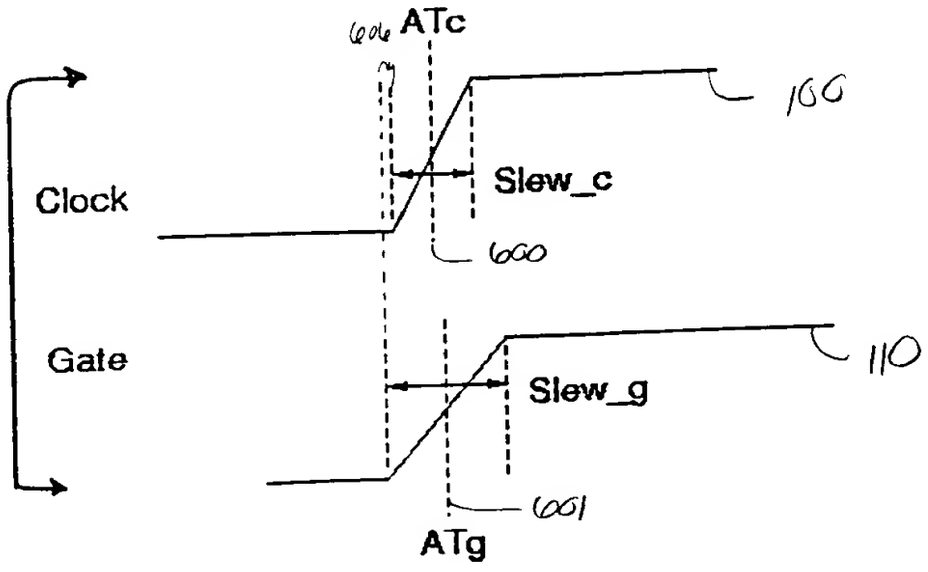
606
ATc
100
Clock
Slew_c
600
110
Gate
Slew_g
601
ATg

FIG. 6B

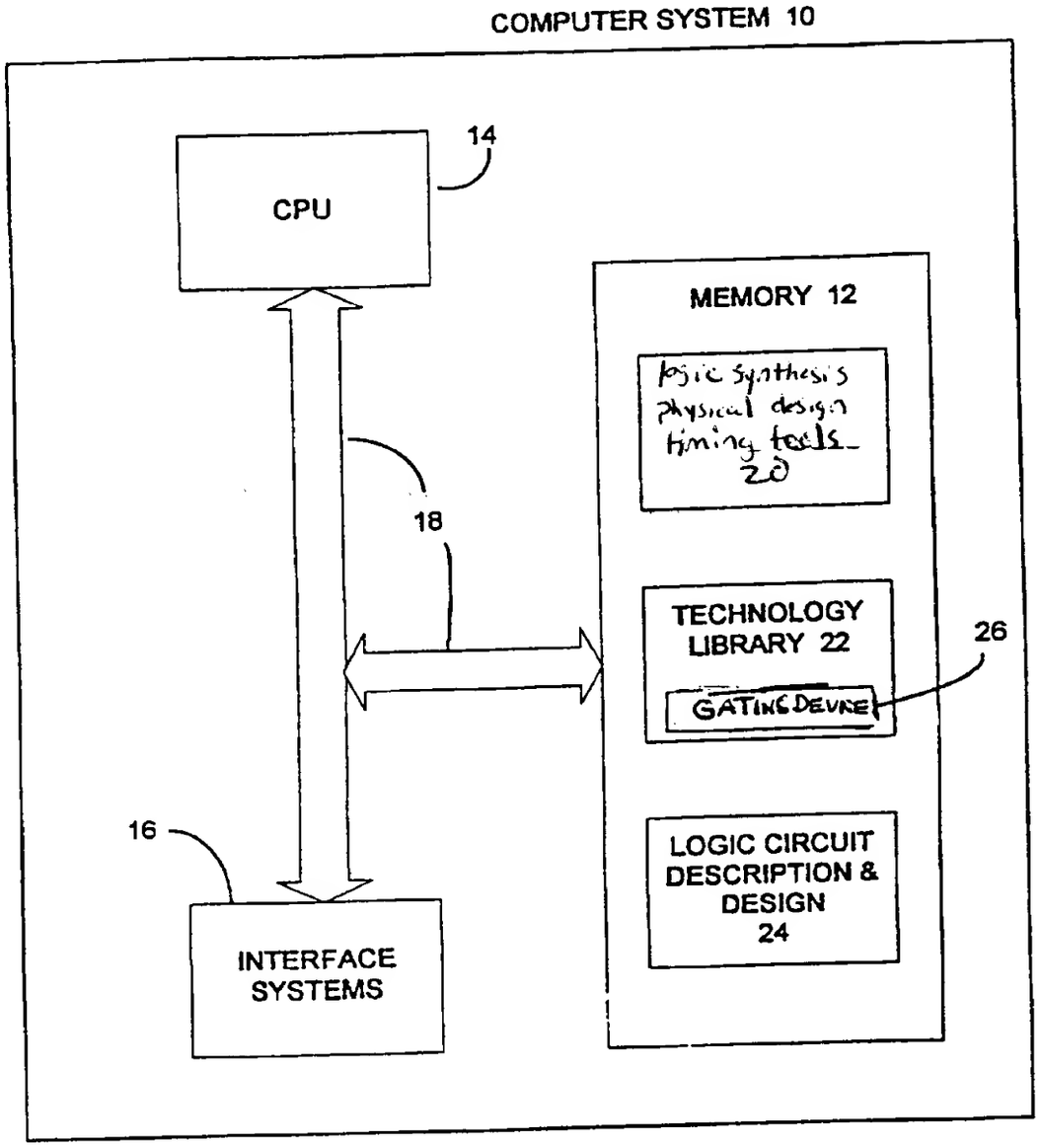
COMPUTER SYSTEM 10
CPU
14
MEMORY 12
logic synthesis
physical design
timing tools
20
18
TECHNOLOGY
LIBRARY 22
GATING DEVICE
26
16
INTERFACE
SYSTEMS
LOGIC CIRCUIT
DESCRIPTION &
DESIGN
24

FIG. 7

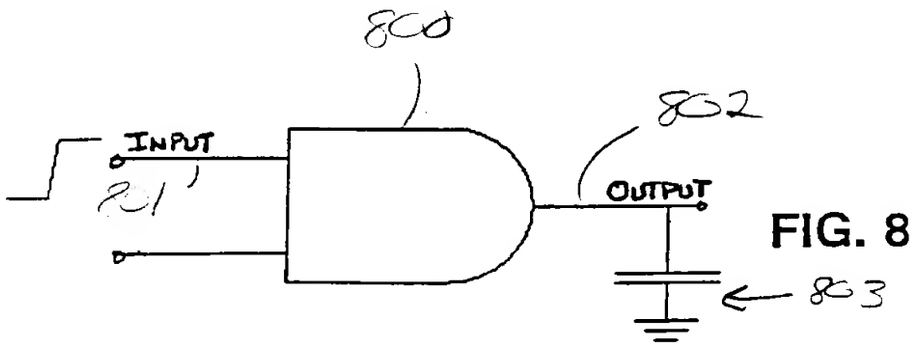
800
802
INPUT
801
OUTPUT
803

FIG. 8

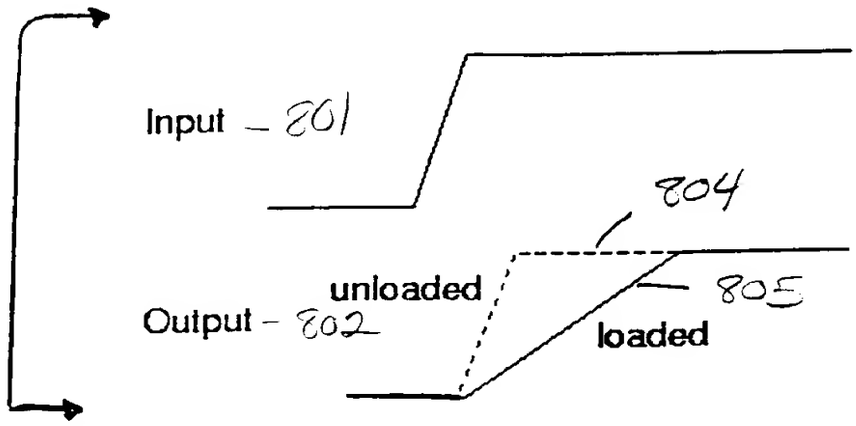
Input – 801
804
unloaded
805
Output – 802
loaded

FIG. 9

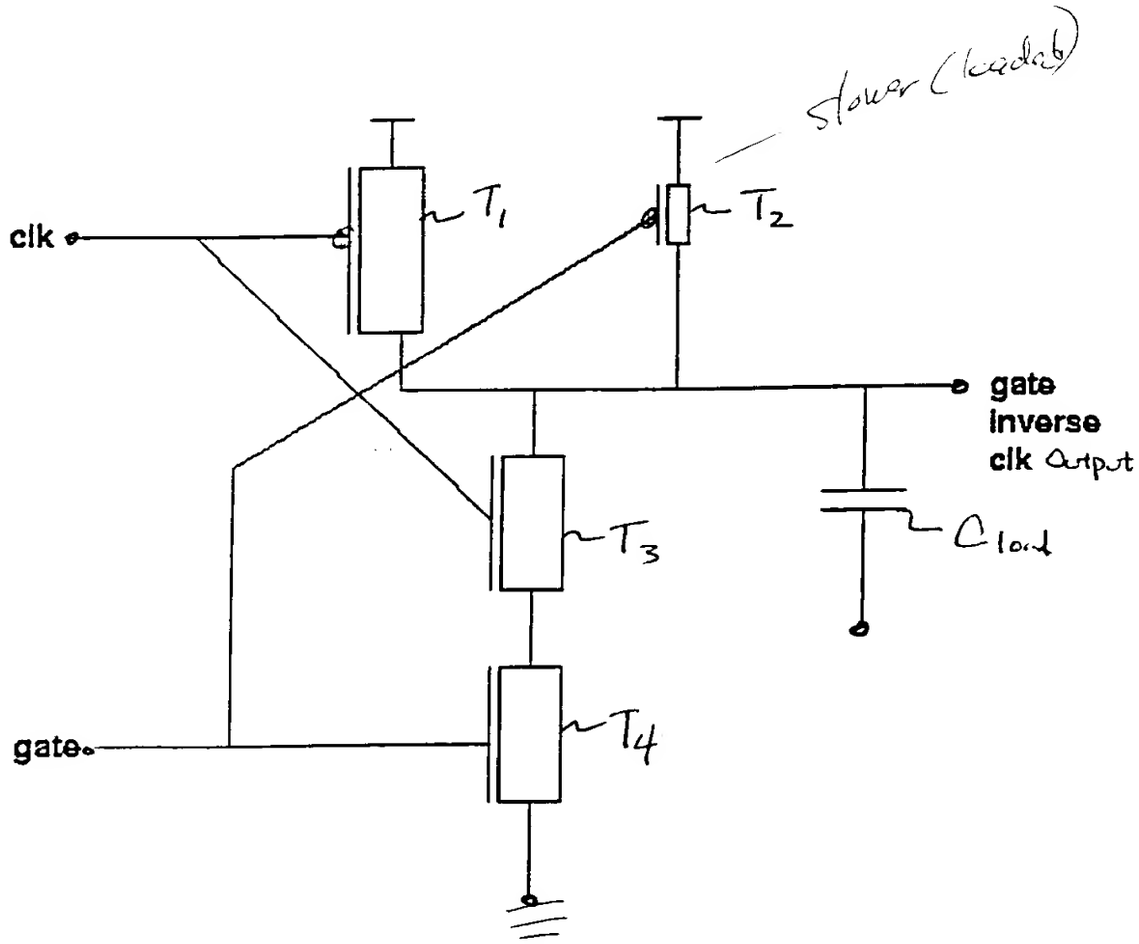
Slower (Headed)
clk
T_1
T_2
gate
inverse
clk output
T_3
C_{load}
gate
T_4

FIG. 10

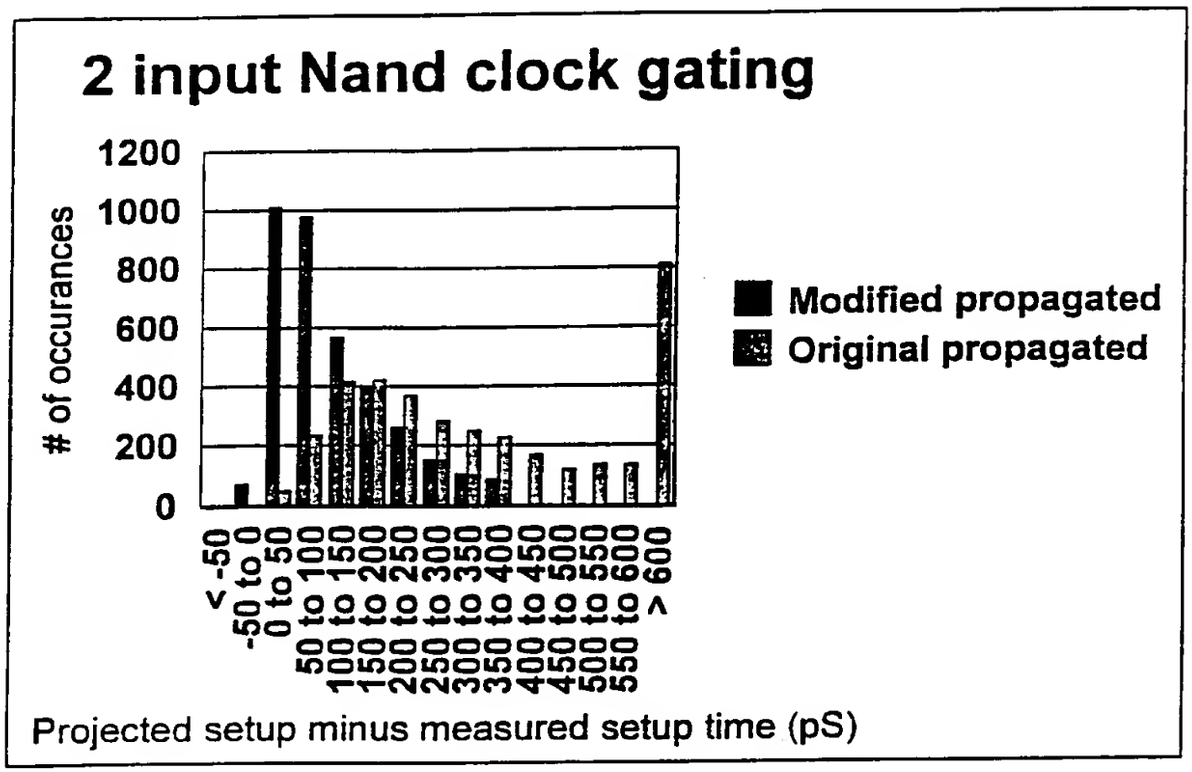
2 input Nand clock gating
# of occurances
1200
1000
800
600
400
200
0
< -50
-50 to 0
0 to 50
50 to 100
100 to 150
150 to 200
200 to 250
250 to 300
300 to 350
350 to 400
400 to 450
450 to 500
500 to 550
550 to 600
> 600
Modified propagated
Original propagated
Projected setup minus measured setup time (pS)

FIG. 11